# **Combinational Circuits**

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The Academic College of Tel-Aviv

January 29, 2025

Transistors

n-ary Gates

Circuits

Seven segment

mod 3

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Bits Adder

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Boolean functions (Platonic world)



Combinational circuits (Real hardware)

### Combinational Circuits

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# Realizing the Boolean Operators

## **Switches**

- A switch is a component having three tips -- --
  - ► One conrol pin
  - ▶ Two data pins
- A switch can be in one of two states
  - ▶ Unpressed • • • The control is at logic 0
- The data pins can be in one of two states
  - ► Connected --- ---
- Naming and drawing convention:
  - ▶ N-switch • Connected ⇔ Pressed
  - ▶ P-switch 📤: Connected ⇔ Unpressed

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# Switch Drawings

| Type       | N             | Р    |
|------------|---------------|------|
| Unpressed  | 0             | 0    |
| switch     |               | ملہ  |
| Pressed    | 1             | 1    |
| switch     | <del></del> - | 00   |
| Bipoloar   | _L            | _L   |
| transistor |               | _/ \ |
| FET        | <u></u>       |      |
| transistor |               |      |

Used in drawings

 $Switches \equiv Transistors$ 

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The following implementation of logic gates is an abstraction of the CMOS technology. The CMOS technology was invented at Fairchild Semiconductor by Frank Wanlass and Chih-Tang Sah.

### **CMOS**

Complementary Metal-Oxide-Semiconductor

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## Gates

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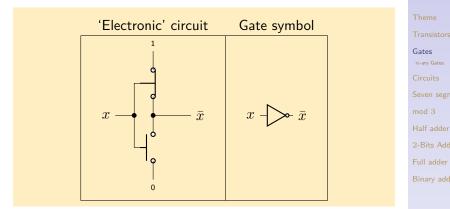
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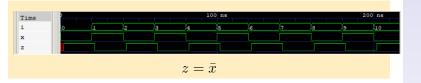
# Logic Gates

Realizing the Operators  $\cdot,\,+$  and  $^-$ 

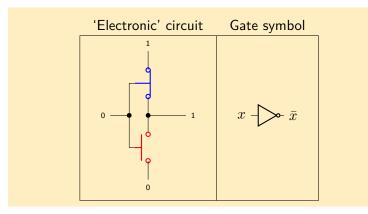
Later on we will see that there are more gates

## Not Gate





# Not Gate x = 0

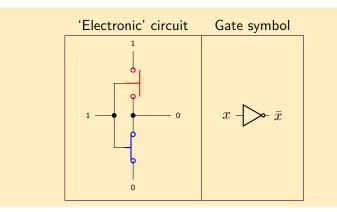


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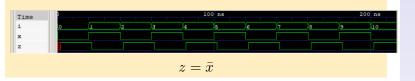
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2-Bits Adder
Full adder
Binary adder



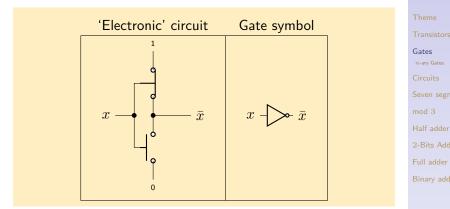
## Not Gate x = 1

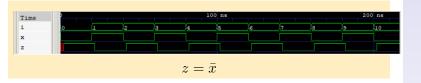


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## Not Gate







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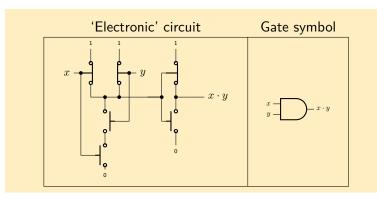
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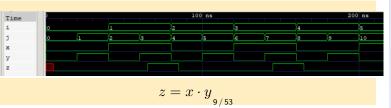
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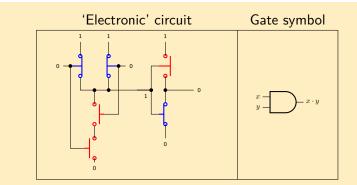
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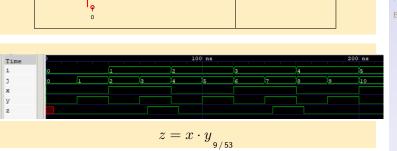
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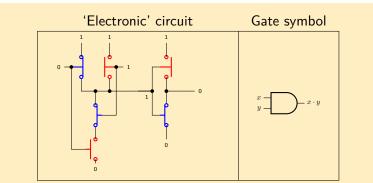
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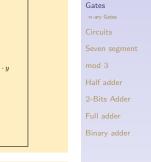
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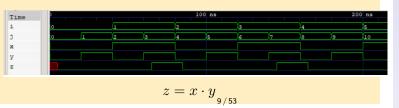
# And Gate x = 0, y = 1

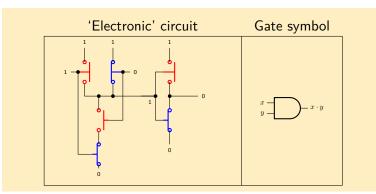
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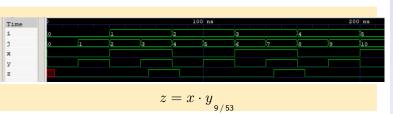
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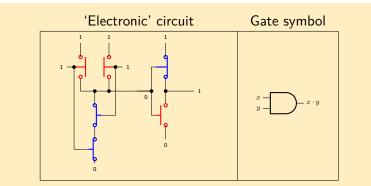
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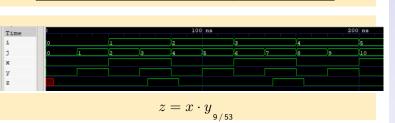
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 $n ext{-ary Gates}$ 

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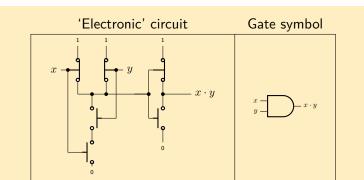
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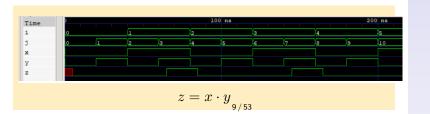
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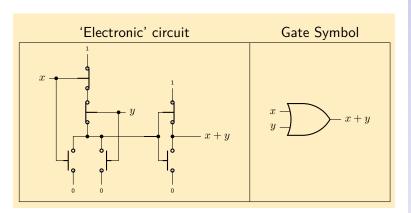
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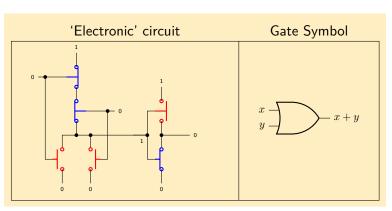
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### Gates





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### Gates

n-ary Gates

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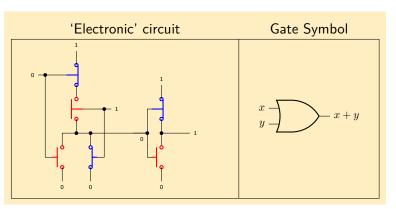
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n-ary Gates

#### Circuits

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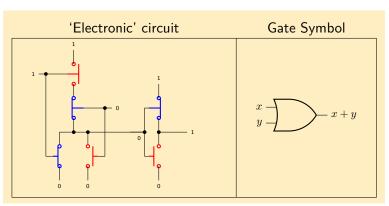
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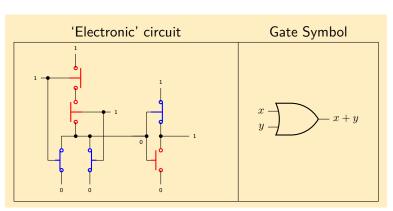
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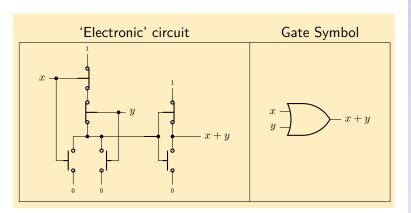
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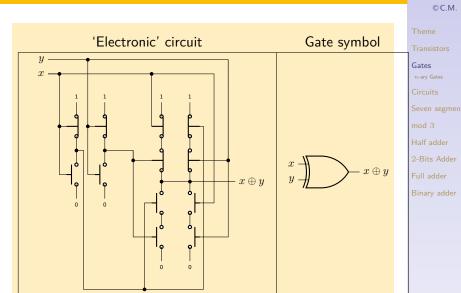




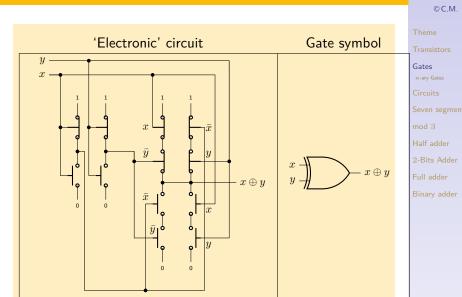
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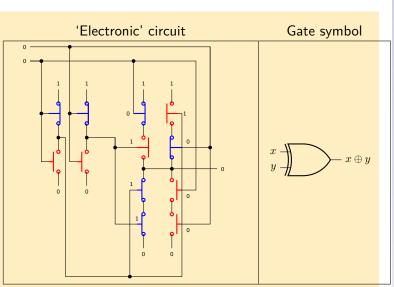


# Xor gate (good place as any)



# Xor gate





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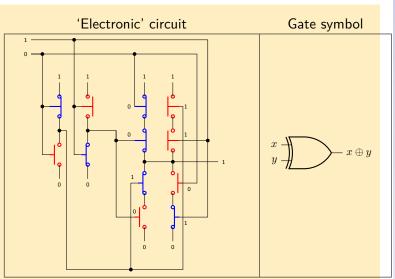
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# $\text{ Xor gate } x = 0, \quad y = 1$



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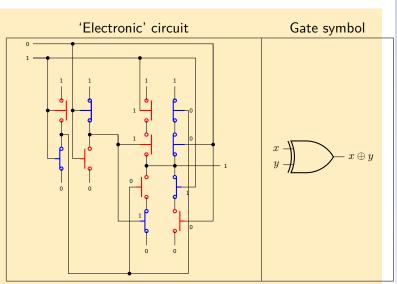
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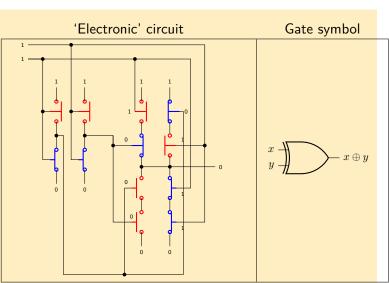
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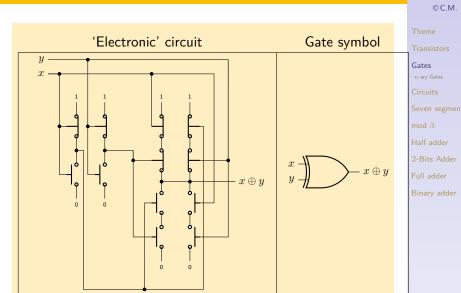
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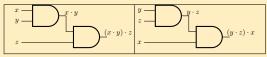
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# Xor gate (good place as any)

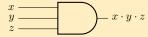


# Commutativity and Associativity

- ullet  $\cdot$ , + and  $\oplus$  are commutative: Gate inputs are symmetric
- $\bullet$  ·, + and  $\oplus$  are associative: Gatewise we get, e.g.,



Or we can use gate with three inputs, e.g.,



- There is a performance **hit** for each additional input pin
- Usually, two successive gate are slower

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# Multi Inputs Gates

| And gate | $x_0$ $x_0$ $x_0$ $x_0$ $x_0$ $x_0$  |
|----------|--------------------------------------|
| Or gate  | $x_0$ $x_0 + \cdots + x_n$           |
| Xor gate | $x_0$ $x_0 \oplus \cdots \oplus x_n$ |

• Most technologies allow at most 5 input pins

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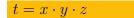
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# 3-Inputs Gates waveforms

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## t = x + y + z



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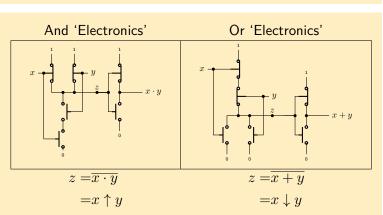
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# 'Electronics' observation regarding gates

The realization of both  $\bigcirc$  and  $\bigcirc$  have  $\triangleright$  at their end



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# Nand $(\uparrow)$ and Nor $(\downarrow)$ Properties

| Nand  | Nor   |
|---|---|
| $\bar{x} = \overline{x \cdot x} = x \uparrow x$ | $\bar{x} = \overline{x+x} = x \downarrow x$     |
| $x \cdot y = \overline{\overline{x \cdot y}} =$ | $x \cdot y = \overline{\overline{x \cdot y}} =$ |
| $=\overline{x \uparrow y} =$                    | $=\overline{\bar{x}+\bar{y}}=$                  |
| $= (x \uparrow y) \uparrow (x \uparrow y)$      | $=(x\downarrow x)\downarrow (y\downarrow y)$    |
| $x + y = \overline{\overline{x + y}} =$         | $x + y = \overline{\overline{x + y}} =$         |
| $=\overline{\bar{x}\cdot\bar{y}}=$              | $=\overline{x\downarrow y}=$                    |
| $= (x \uparrow x) \uparrow (y \uparrow y)$      | $=(x\downarrow y)\downarrow (x\downarrow y)$    |

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# Complete System

### Definition

A set of functions and constants is a complete system if every boolean function can be defined with them

# Corollary

Both  $\{\uparrow\}$  and  $\{\downarrow\}$  are complete systems.

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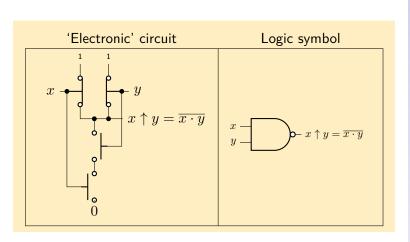
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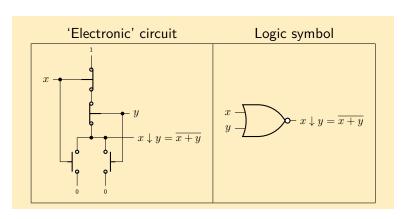
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#### Gates



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| Gate              | Nand   | Nor  |
|-------------------|--|--|
| x — — — $\bar{x}$ | $x \uparrow x = \bar{x}$   | $x \rightarrow x \downarrow x = \bar{x}$   |
|                   | $\begin{array}{c c} x & & \\ y & & \\ \end{array}$   | $x - (x \downarrow x) \downarrow \\ y - (y \downarrow y) = \\ x \cdot y$   |
| x - y - x + y     | $\begin{array}{c} x \\ y \\ \end{array} \begin{array}{c} (x \uparrow x) \uparrow \\ (y \uparrow y) = \\ x + y \end{array}$ | $ \begin{array}{c} x \longrightarrow \\ y \longrightarrow \\ \end{array} $ $ \begin{array}{c} (x \downarrow y) \downarrow \\ (x \downarrow y) = \\ x + y \end{array} $ |

Realization of XOR should be here

#### Gates

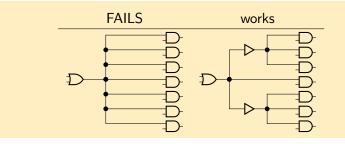
#### Two final gates

• The buffer gate (important in real circuits):



• The nxor gate:

$$x + y \Rightarrow \overline{x \oplus y}$$



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#### Multi Inputs Variants

#### Associative complement

| Nand gate | $x_0$ $x_0$ $x_0$ $x_0$ $x_0$ $x_0$ $x_0$ |
|-----------|---|
| Nor gate  | $x_0$ $x_0 + \cdots + x_n$                |
| Nxor gate | $x_0$ $x_0 \oplus \cdots \oplus z$        |

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# (Carmi) Lecture 6 reached here

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#### **Combinational Circuits**

(Realization of boolean functions)

Recall that the booean operators are boolean functions

#### Functions to be Realized

Combinational Circuits

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- 2-bit binary adder
- Full adder
- Binary adder

The boolean functions are from the previous chapter

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#### Combinational Circuits

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Seven segment

### Realizing the Seven-Segment

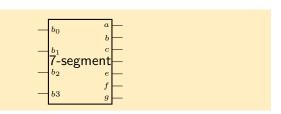
The formuale are from the previous lecture

- 1. Block diagram
- 2. Logic circuit

### Seven-Segment (block diagram)

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### Seven-Segment (formulae)

| <u>SOP</u>  | <u>POS</u>  |                   | Т      |
|---|---|-------------------|--------|
| $a = m_0 + m_2 + m_3 + m_5 + m_7 + m_8 + m_9$             | $a = \bar{m}_1 \bar{m}_4 \bar{m}_6$                     |                   |        |
| $b = m_0 + m_1 + m_2 + m_3 + m_4 + m_7 + m_8 + m_9$       | $b = \bar{m}_5 \bar{m}_6$                               |                   | G      |
| $c = m_0 + m_1 + m_3 + m_4 + m_5 + m_6 + m_7 + m_8 + m_9$ | $c = \bar{m}_2$   |                   |        |
| $d = m_0 + m_2 + m_3 + m_5 + m_6 + m_8$                   | $d = \bar{m}_1 \bar{m}_4 \bar{m}_7$                     |                   |        |
| $e = m_0 + m_2 + m_6 + m_8$                               | $e = \bar{m}_1 \bar{m}_3 \bar{m}_4 \bar{m}_5 \bar{m}_7$ | $\bar{m}_{arphi}$ | 5<br>9 |
| $f = m_0 + m_4 + m_5 + m_6 + m_8 + m_9$                   | $f = \bar{m}_1 \bar{m}_2 \bar{m}_3 \bar{m}_7$           |                   | n      |
| $g = m_2 + m_3 + m_4 + m_5 + m_6 + m_8 + m_9$             | $g = \bar{m}_0 \bar{m}_1 \bar{m}_7$                     |                   | H      |
|   |   |                   | 2      |

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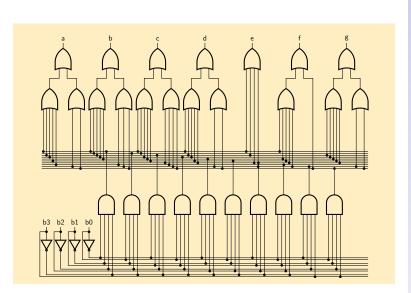
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## Seven Segment (SOP)



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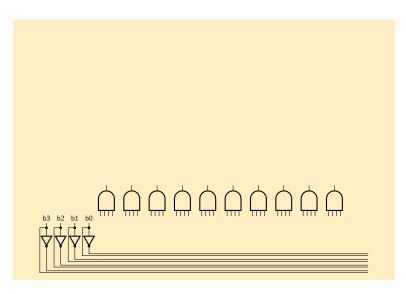
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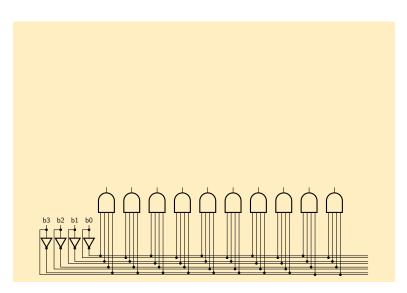
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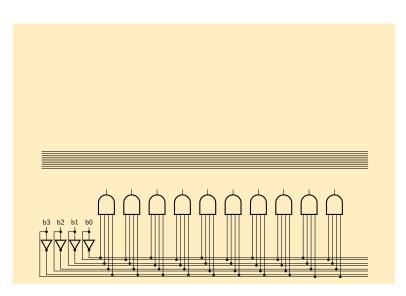
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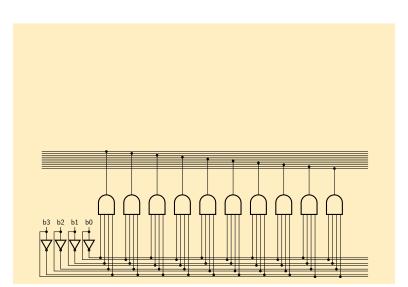
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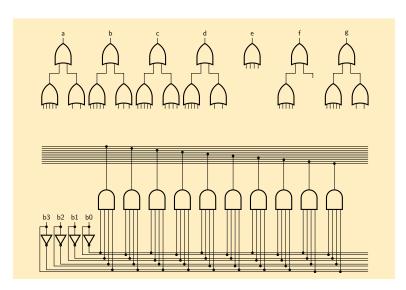
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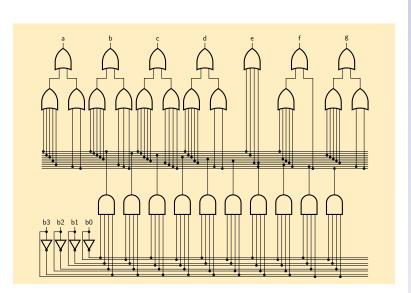
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## Seven Segment (SOP)



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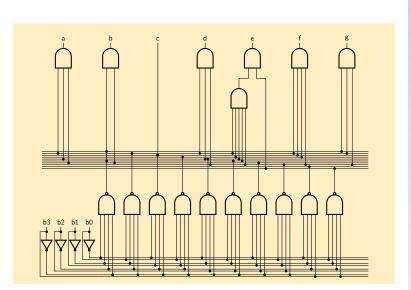
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## Seven Segment (POS)



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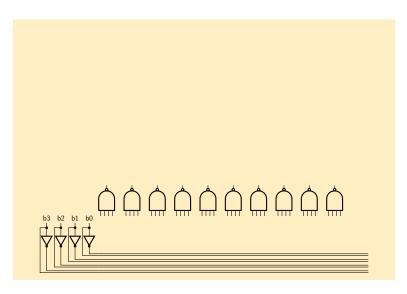
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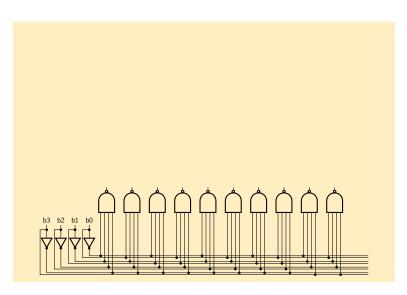
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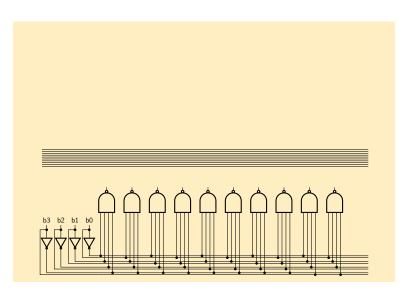
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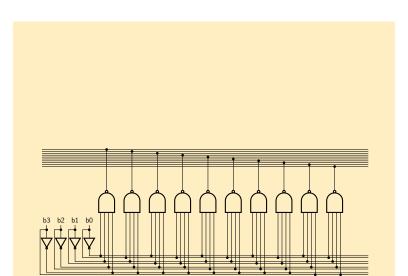
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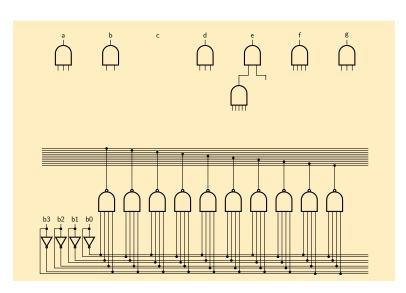
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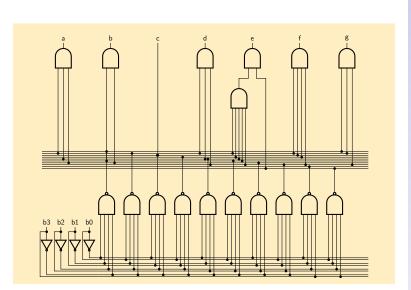
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## Seven Segment (POS)



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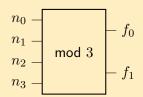
## Realizing mod 3

The formuale are from the previous lecture

- 1. Block diagram
- 2. Logic circuit

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mod 3 Block Diagram



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$$f_1 = \bar{n}_3 \bar{n}_2 n_1 \bar{n}_0 + \bar{n}_3 n_2 \bar{n}_1 n_0 + n_3 \bar{n}_2 \bar{n}_1 \bar{n}_0 + n_3 \bar{n}_2 n_1 n_0 + n_3 n_2 n_1 \bar{n}_0$$

$$f_0 = \bar{n}_3 \bar{n}_2 \bar{n}_1 n_0 + \bar{n}_3 n_2 \bar{n}_1 \bar{n}_0 + \bar{n}_3 n_2 n_1 n_0 + n_3 \bar{n}_2 n_1 \bar{n}_0 + n_3 n_2 \bar{n}_1 n_0$$

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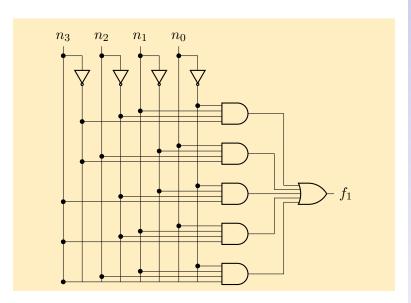
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#### $mod 3 f_1$ -Circuit



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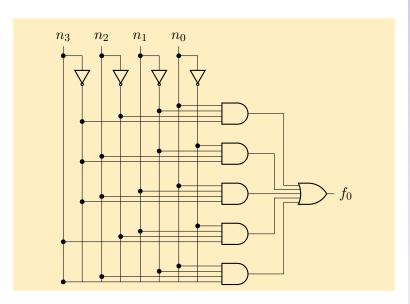
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## $\mod 3$ $f_0$ -Circuit



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Half adder

## Realizing the Half Adder

The formuale are from the Boolean Algebra lecture

- 1. Block diagram
- 2. Logic circuit

#### Half Adder (previous lecture)

$$f_1 = x \cdot y$$
$$f_0 = x \oplus y$$

#### Two bits in, two bits out



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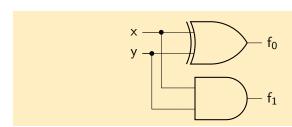
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## Realizing 2-Bits Adder

(The formulae are from the Boolean Algebra chapter)

$$f_{2} = \bar{x}_{1}x_{0}y_{1}y_{0} + x_{1}\bar{x}_{0}y_{1}\bar{y}_{0} + x_{1}\bar{x}_{0}y_{1}y_{0} + x_{1}x_{0}\bar{y}_{1}y_{0} + x_{1}x_{0}\bar{y}_{1}y_{0} + x_{1}x_{0}y_{1}\bar{y}_{0} + x_{1}x_{0}y_{1}y_{0}$$

$$f_{1} = \bar{x}_{1}\bar{x}_{0}y_{1}\bar{y}_{0} + \bar{x}_{1}\bar{x}_{0}y_{1}y_{0} + \bar{x}_{1}x_{0}\bar{y}_{1}y_{0} + \bar{x}_{1}x_{0}y_{1}\bar{y}_{0} + x_{1}x_{0}\bar{y}_{1}\bar{y}_{0} + x_{1}x_{0}y_{1}y_{0} + x_{1}x_{0}y_{1}\bar{y}_{0} + x_{1}x_{0}y_{1}\bar{y}_{0} + \bar{x}_{1}\bar{x}_{0}y_{1}y_{0} + \bar{x}_{1}x_{0}y_{1}\bar{y}_{0} + \bar{x}_{1}x_{0}y_{1}\bar{y}_{0} + x_{1}\bar{x}_{0}y_{1}\bar{y}_{0} + x_{1}\bar{x}_{0}y_{1}\bar{y}_{0} + x_{1}\bar{x}_{0}y_{1}\bar{y}_{0} + x_{1}\bar{x}_{0}y_{1}\bar{y}_{0} + x_{1}x_{0}y_{1}\bar{y}_{0}$$

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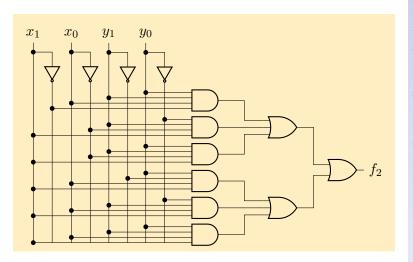
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### 2-Bits Adder $f_2$ -Circuit



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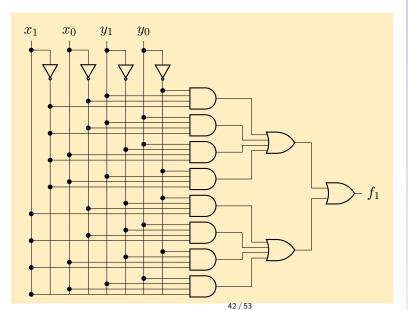
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## 2-Bits Adder $f_1$ -Circuit

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# 2-Bits Adder $f_0$ -Circuit

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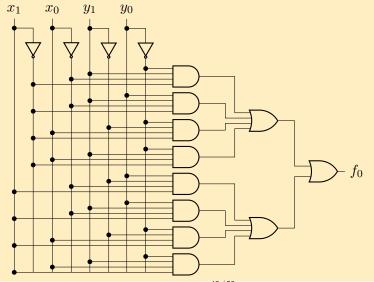
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# Realizing the Full Adder

Formuale are from the boolean algebras lecture

- 1. Block diagram
- 2. Logic circuit

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$$f_0(x, y, z) = x \oplus y \oplus z$$

$$f_1(x, y, z) = \bar{x}yz + x\bar{y}z + xy\bar{z} + xyz =$$

$$= (x + y + z)(x + y + \bar{z})(x + \bar{y} + z)(\bar{x} + y + z) =$$

$$= yz + xz + xy$$

Transistors

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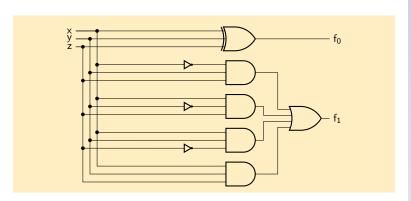
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Half adde

2-Bits Adder

Full adder

## Full adder ( $f_1$ SOP)



$$f_0(x, y, z) = x \oplus y \oplus z$$
  
$$f_1(x, y, z) = \bar{x}yz + x\bar{y}z + xy\bar{z} + xyz$$

#### Theme

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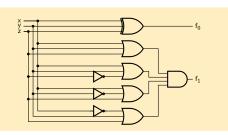
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2-Bits Adder

Full adder

## Full adder ( $f_1$ POS circuits)



$$f_0(x, y, z) = x \oplus y \oplus z$$
  
 $f_1(x, y, z) = (x + y + z)(x + y + \bar{z})(x + \bar{y} + z)(\bar{x} + y + z)$ 

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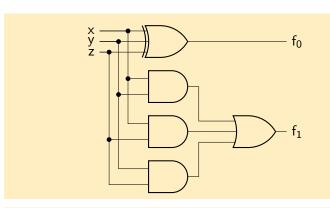
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## Full adder (simplified circuit)



$$f_0(x, y, z) = x \oplus y \oplus z$$
  
$$f_1(x, y, z) = yz + xz + xy$$

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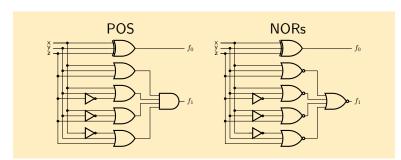
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$$f_0(x, y, z) = x \oplus y \oplus z$$
  
 $f_1(x, y, z) = (x + y + z)(x + y + \bar{z})(x + \bar{y} + z)(\bar{x} + y + z)$ 

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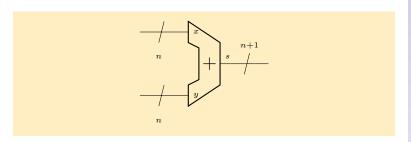
Binary adder

## Realizing the Binary Adder

The formuale are from the previous lecture

- 1. Block diagram
- 2. Logic circuit

# Binary adder (block diagram)



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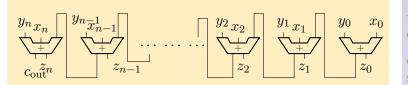
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## Binary Adder (circuit)



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