Instruction Set Architecture (ISA)

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Major ISA types

- CISC : Complext Instruction Set Computer
- RISC : Reduced Instruction Set Computer

In hindsight maybe RISC should have been named

- SISC: Simple instruction Set Computer

It just happends that some RISC computers have an awfull lot of instructions

Load-Store Machine

These are machines in which

- Few dedicated instructions access memory
- All the other instructions work between registers

It seems modern RISC machines are all of this type

RISCV 64

ARM

PDP-11 (Made by DEC, may it rest in peace)

- This was the first computer I used or even seen
- It occupied a (small) room
- It was love at first sight 
- DEC wrote for it the following OSes: RT-11, RSTS/E, RSX-11(B,C,D,M), RSX-11M-PLUS
- AT&T, unknowingly, wrote for it the Unix OS (v6 is the **famous** one)

History

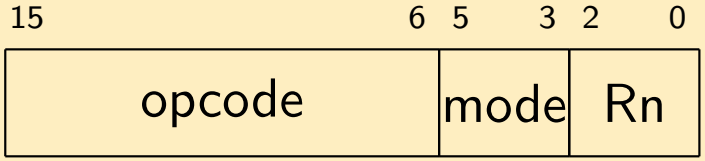
- The first PDP-11 appeared at 1969
- The last probably at the 1990s
- It has a very very elegant instruction set
- The number of instructions is small
- The number of instruction family is very small
- The operands make this a CISC machine

General Characteristics

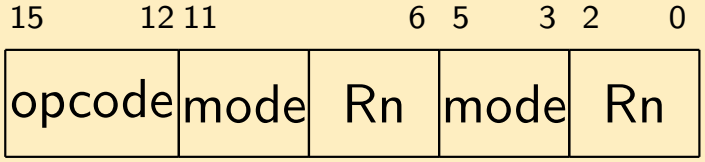
Years	1970-80's
ISA type	CISC
Regularity	Very regular
Word size	16b
GPRs	6

Familes

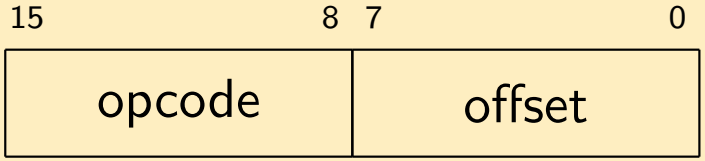
- Single Operand



- Double operand:



- Branches:



Single Operand

INC(B)
DEC(B)
NEG(B)
NOP
TST(B)
ASR(B)
ASL(B)
ROR(B)
ROL(B)
SWAB
ADC(B)
SBC(B)
SXT

Double Operand

MOV
ADD
SUB
CMP(B)
ASH
ASHC
MUL
DIV
BIT(B)
BIC(B)
BIS(B)
XOR

Registers

R0	
R1	
R2	
R3	
R4	
R5	
R6	SP
R7	PC

Addressing Modes

		DEC	Unix
Mode	Name	assembly	assembly
0	Register	Rn	Rn
1	Register deferred	(Rn)	(Rn)
2	Autoincrement	(Rn)+	(Rn)+
3	Autoincrement deferred	@(Rn)+	*(Rn)+
4	Autodecrement	-(Rn)	-(Rn)
5	Autodecrement deferred	@-(Rn)	*-(Rn)
6	Index	X(Rn)	X(Rn)
7	Index deferred	@X(Rn)	*X(Rn)

VAX